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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,229	WARD, WILLIAM P.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *2-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-24,26,28,30,32,33,40 and 44* is/are rejected.

7)☒ Claim(s) *25,27,29,31,34-39 and 41-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is taken in response to Applicant's communication filed June 7, 2004 responding to the Official Action/Rejection dated March 4, 2004. The Applicant's arguments and/or amendments have been considered with the results that follow.

2. Claims 1 and 5-44 are pending in the application examination.

Response to Arguments

3. Applicant's arguments filed June 7, 2004 have been fully considered but they are not deemed to be persuasive for at least the following remarks.

Claims 10-15 and 20-22 were and stand rejected under 35 USC 102 over US 6,480,941 (Franke). Applicant argued that the reference does not anticipate independent claim 10 for the fact that Franke describes a memory partitioning system. Applicant argued that multiple memory control interfaces cannot be connected to the same internal bus as that would violate the partitioning and isolation sought by the Franke partition arrangement, i.e., Franke fails to meet the claimed limitation "a plurality of memory controllers connected to a first one of a plurality of memory buses". In contrast, it is contended that Franke specifically meet the requirement as Franke discloses, "All system components that are attached via the bus coupling of the same internal bus belong to a partition" (Col. 4, Lines 62-64). If applicant's line of reasoning with respect to multiple memory control interfaces cannot be connected to the same

internal bus was accurate, arbitration would not be a factor in Franke's arrangement. Franke's system provides several ports to accept memory requests from different sources at a time.

Applicant argued that Franke discloses "it is imperative that the crossbar switch must be programmed in such a manner that each EC_j is coupled with at most one IB_i to avoid a single system component (CPU, I/0 Controller) being seen by more than one partition" and further states that, because of this teaching, multiple memory control interfaces cannot be connected to the same internal bus as that would violate the partitioning and isolation sought by the Franke partition arrangement. In contrast to applicant line of reasoning, Franke's teaching is to apply coherency protocol as it is imperative to arbitrate between multiple requests received at a given time to provide proper service of load and store requests (Col. 5, Lines 1-7). Franke's system teaches "Once all the bus coupling devices (210) have been programmed and the partitions have been successfully setup, all system components (101,102) connected to the EC_j of the crossbar switch that have the EC_j coupled to the same IB_i belong to the same partition" (Col. 6, Lines 26-30). With this teaching it is clear that multiple controllers or bus control interfaces are connected with one single bus, as required in the claims. The one-to-one correspondence between a memory control interface and in internal bus would not violate the partitioning system as Franke teaches dynamic assignment and re-assignment of the memory port of memory partition with active and inactive state of the bus coupling device (Col. 6, Lines 45-52).

Applicant argued that Franke fails to teach each memory controller interface does not monitor memory requests generated by each other but admits that Franke teaches the memory control interfaces 280 snooping on a respective internal bus IB for memory operations. However, it addition to the admission, Franke teaches that a standard memory controller interface has to detect and accept memory operations within its snoop logic (550), the memory controller interface has to implement the proper bus protocol by snooping on the bus for memory transactions, and forwards the memory operations to the memory controller (return to the requestor) [Col. 7, Lines 29-45]. Unlike in the statement of applicant's remarks, the memory controller interface responds to requests (not the memory controller) and if an operation does not yield in a hit the memory controller interface does not respond to the operation and does not assert the necessary signal on the internal bus (Col. 8, Lines 8-10).

Claims 1, 5-9, 16-19, 23, 24, 26, 28, 30, 32, 33, 40, and 44 were rejected under 103 over Franke in view of Xanthaki, and applicant argued that Franke fails to disclose plurality of memory controllers able to generate memory requests on the same bus. It has been shown above that applicant is not convincing as Franke clearly teaches plurality of memory controller interface generating memory transactions snooping the memory transaction on a common bus. A prima facie case of obviousness has been established and as Franke's system teaches arbitration between multiple requests on a single bus and Xanthaki discloses bus interface protocol and priority scheme defining interleaving arrangements for request by multiple controllers on a memory bus. Although time slot priority is a known principle of RAMBUS channels (Section 2.2 of

Xanthaki), Xanthaki discloses RAMBUS Channel accesses with interleaving capability according to time slot schedules. A request that results in a miss is completed at the end of the acknowledge window where the master would have to wait for the Read/Write MissDelay cycles before reissuing the request.

Because applicant remarks are not convincing enough to withdraw the rejection and because above remarks have addressed applicant's concerns, the previously applied rejection is maintained and repeated below.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 10-15 and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,480,941 (Franke et al).

With respect to claims 10 and 15, Franke discloses a system comprising: a plurality of memory buses (*set of internal system buses*); a hub connected to the plurality of memory buses (*configurable crossbar switch; multi-port memory controller*); and a plurality of memory controllers connected to a first one the memory buses (*associated with each port is a memory controller interface*) [Col. 4, Lines 35-54] each memory controller to monitor memory requests generated by another memory controller in performing

memory related actions (*each memory controller interface snooping on the bus for memory operations*) [Col. 5, Lines 1-7; Col. 7, Lines 29-33], the memory controllers to access a second one of the memory buses through the hub (the memory controllers to access a different partition associated with a particular internal bus [Col. 4, Lines 59-64].

With respect to claims 13-14, and 20, Franke discloses the memory related action comprising a memory requests and each memory controller to determine if the memory buses are available based on outstanding requests from other memory controllers (*external bus or components can be attached to one internal bus at a time*) [Col. 4, Lines 60-64].

With respect to claims 11-12 and 21-22, Franke teaches the memory related action comprising read-modify-write transaction or a cache coherency action (*each memory controller interface having snooping logic snooping on the bus for memory transaction where snooping on the bus is part of its cache coherence protocol*) [Col. 7, Lines 29-46; Col. 5, Lines 2-5].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5-9, 16-19, 23-24, 26, 28, 30, 32-33, 40 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,480,941 (Franke et al) in view of Xanthaki (A Memory Controller for Access Interleaving over a Single Rambus).

With respect to claims 1, 16, 17 and 23, Franke teaches the invention as claimed, where external bus or components can be attached to one internal bus at a time, implementing a priority scheme [Col. 4, Lines 60-64], but fails to define time slot priority associated with the controllers. However, Franke discloses the invention with the principle of Rambus channel where no master can write to a channel until another write is completed, the system arbitrates among the multiple port to provide proper service of load and store. Xanthaki discloses interleaving capability of the Rambus Channel Access according to a scheduling algorithm, such that a request resulting in a miss is completed at the end of the acknowledge window where the master would have to wait for the Read/Write MissDelay cycles before reissuing the request (Section 2.2). Therefore, it would have been obvious to implement the priority scheme into the teaching by Franke because access interleaving would have permitted request scheduling while achieving high bandwidth. Xanthaki discusses access interleaving and how it effects on memory controller where the controller must ensure that there will be no conflicts on the Rambus channel by scheduling the requests and data packets in proper bus cycles. For a new request issued in the middle of some previous transaction, the controller should know the state of the Rambus channel: which time slots are free and which are reserved.

With respect to claims 5-9, 18-19, 24, 26, 28, 30, 32-33, 40 and 44, the combination of Franke and Xanthaki teaches the invention defining time-slot and request select priority scheme, with multiple controller able to concurrently generate requests to a particular bus associated with a particular partition [Col. 4, Lines 47-64].

Allowable Subject Matter

8. Claims 25, 27, 29, 31, 34-39 and 41-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

August 3, 2004

PIERRE BATAILLE
PRIMARY EXAMINER